What is Claimed:

1. A multi chip module substrate comprising:

a plurality of chip sites each having:

(a) a plurality of signal vias, and

(b) a plurality of repair vias;

a circuit line net having a plurality of circuit lines, each said circuit line extending between and intended to electrically connect selected signal vias; and

a repair line net having a plurality of groups of repair lines, each said repair line extending between and electrically connecting a repair via of one said chip site and a repair via of another said chip site.

2. A multi chip module substrate according to claim 1 wherein said circuit lines are within said chip sites and said repair lines are within said chip sites.

3. A multi chip module substrate according to claim 1 wherein said repair vias are outside of and surrounding an array of said signal vias.

4. A multi chip module substrate according to claim 3 wherein said chip sites are identical.

5. A multi chip module substrate according to claim 1 wherein said repair vias are disposed uniformly outside of and surrounding an array of said signal vias.

6. A multi chip module substrate according to claim 5 wherein said chip sites are identical.

7. A multi chip module substrate according to claim 1 further including:

(a) a first jumper connection extending between and electrically connecting a first signal via in a first chip site and that repair via in said first chip site that is connected to a repair via in a second chip site in which a second signal via is located and to which said first signal via is intended to be connected; and

(b) a second jumper connection extending between and electrically connecting said second signal via in said second chip site and that repair via in said second chip site that is connected to said repair via in said first chip site to which said first signal via is electrically connected.

8. A multi chip module substrate according to claim 7 wherein said circuit lines are within said chip sites and said repair lines are within said chip sites.

9. A multi chip module substrate according to claim 7 wherein said repair vias are outside of and surrounding an array of said signal vias.

10. A multi chip module substrate according to claim 9 wherein said chip sites are identical.

11. A multi chip module substrate according to claim 7 wherein said repair vias are disposed uniformly outside of and surrounding an array of said signal vias.

12. A multi chip module substrate according to claim 11 wherein said chip sites are identical.

13. A multi chip module substrate according to claim 1 wherein:

(a) the number of said repair vias in each said chip site is equal to the number of said chip sites minus one,

(b) the number of said groups of said repair lines is equal to the number of said chip sites, and

(c) the number of said repair lines in each said group is equal to the number of said chip sites minus one.

14. A multi chip module substrate according to claim 4 wherein:

(a) the number of said repair vias in each said chip site is equal to the number of said chip sites minus one,

(b) the number of said groups of said repair lines is equal to the number of said chip sites, and

(c) the number of said repair lines in each said group is equal to the number of said chip sites minus one.

15. A multi chip module substrate according to claim 7 wherein:

(a) the number of said repair vias in each said chip site is equal to the number of said chip sites minus one,

(b) the number of said groups of said repair lines is equal to the number of said chip sites, and

(c) the number of said repair lines in each said group is equal to the number of said chip sites minus one.

16. A method of repairing an electronic package comprising the steps of:

providing a multi chip module substrate including:

(a) a plurality of chip sites each having:

(1) plurality of signal vias, and

(2) plurality of repair vias,

(b) a circuit line net having a plurality of circuit lines, each said circuit line extending between and intended to electrically connect selected signal vias, and

(c) a repair line net having a plurality of groups of repair lines, each said repair line extending between and electrically connecting a repair via of one said chip site and a repair via of another said chip site;

identifying in a circuit intended to be composed of:

(a) a first signal via in a first chip site,

(b) a second signal via in a second chip site, and

(c) a circuit line extending between and intended to electrically connect said first signal via and said second signal via

a defect in one of:

(a) said first signal via,

(b) said second signal via, and

(c) said circuit line extending between and intended to electrically connect said first signal via and said second signal via;

isolating said first signal via;

isolating said second signal via;

electrically connecting said first signal via in said first chip site to that repair via in said first chip site that is connected to a repair via in said second chip site; and

electrically connecting said second signal via in said second chip site to that repair via in said second chip site that is connected to said repair via in said first chip site connected to said first signal via.

17. A method of repairing an electronic package according to claim 16 wherein:

(a) the step of isolating said first signal via includes depositing a thin dielectric over said first signal via,

(b) the step of isolating said second signal via includes depositing a thin dielectric over said second signal via,

(c) the step of electrically connecting said first signal via in said first chip site to that repair via in said first chip site that is connected to a repair via in said second chip site includes depositing a first jumper conductor between said first signal via in said first chip site and that repair via in said first chip site that is connected to a repair via in said second chip site; and

(d) the step of electrically connecting said second signal via in said second chip site to that repair via in said second chip site that is connected to said repair via in said first chip site connected to said first signal via includes depositing a second jumper conductor between said second signal via in said second chip site and that repair via in said second chip site that is connected to a repair via in said first chip site.

18. A method of repairing an electronic package according to claim 17 wherein:

(a) the step of electrically connecting said first signal via in said first chip site to that repair via in said first chip site that is connected to a repair via in said second chip site further includes overcoating said first jumper conductor with a dielectric, and

(b) the step of electrically connecting said second signal via in said second chip site to that repair via in said second chip site that is connected to said repair via in said first chip site further includes overcoating said second jumper conductor with a dielectric.

19. A method of repairing an electronic package according to claim 18:

(a) wherein each of said chip sites further includes a ceramic base into which said signal vias and said repair vias extend, and

(b) said method further includes the step of firing the electronic package to bond:

(1) said thin dielectric over said first signal via to said first signal via,

(2) said thin dielectric over said second signal via to said second signal via,

(3) said first jumper conductor to said ceramic base of said chip site having said first signal via and that repair via of the chip site having said first signal via that is connected to that repair via of the chip site having said second signal via,

(4) said second jumper conductor to said ceramic base of said chip site having said second signal via and that repair via of the chip site having said second signal via that is connected to that repair via of the chip site having said first signal via,

(5) said dielectric overcoating of said first jumper conductor to said first jumper conductor, and

(6) said dielectric overcoating of said second jumper conductor to said second jumper conductor.

20. A method of repairing an electronic package according to claim 19 wherein:

(a) the step of depositing said first jumper conductor includes depositing said first jumper conductor over said thin dielectric over said first signal via,

(b) the step of depositing said second jumper conductor includes depositing said second jumper conductor over said thin dielectric over said second signal via,

(c) the step of overcoating said first jumper conductor with a dielectric includes overcoating said first jumper conductor over said first signal via with said dielectric overcoating said first jumper conductor,

(d) the step of overcoating said second jumper conductor with a dielectric includes overcoating said second jumper conductor over said second signal via with said dielectric overcoating said second jumper conductor, and

(e) said method further includes the steps of:

(1) removing said dielectric overcoating over said first signal via to expose said first jumper conductor over said first signal via, and

(2) removing said dielectric overcoating over said second signal via to expose said second jumper conductor over said second signal via.